

EAST Search History

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L1	31	"5838161"	USPAT	OR	OFF	2006/04/27 19:31
L3	61	(US-20050224792-\$ or US-20060019414-\$ or US-20020098681-\$).did. or (US-6822260-\$ or US-6815319-\$ or US-6790685-\$ or US-6600333-\$ or US-6620635-\$ or US-5561373-\$ or US-4516071-\$ or US-6650129-\$ or US-6995392-\$ or US-6894520-\$ or US-6822437-\$ or US-6747445-\$ or US-6525548-\$ or US-6563320-\$ or US-6559475-\$ or US-6144040-\$ or US-6403389-\$ or US-6362638-\$ or US-6343370-\$ or US-6057171-\$ or US-6111269-\$ or US-6087189-\$ or US-5963784-\$ or US-6055858-\$ or US-6022750-\$ or US-5663651-\$). did. or (US-5990567-\$ or US-5949547-\$ or US-5838161-\$ or US-4896108-\$ or US-5835161-\$ or US-5640097-\$ or US-5608285-\$ or US-4672314-\$ or US-5552718-\$ or US-4855253-\$ or US-3650020-\$ or US-4386459-\$ or US-4347479-\$ or US-3974443-\$ or US-5834795-\$ or US-6150669-\$ or US-4978923-\$ or US-4871962-\$ or US-4399205-\$ or US-5247262-\$ or US-4835466-\$ or US-5051690-\$ or US-6921672-\$ or US-6570181-\$ or US-5661345-\$ or US-6897475-\$ or US-5952674-\$). did. or (US-6831365-\$ or US-6835578-\$ or US-6768323-\$ or US-6320391-\$ or US-6218848-\$). did.	US-PGPUB; USPAT	OR	OFF	2006/04/27 20:12
L4	6	3 and akram	USPAT	OR	OFF	2006/04/27 20:12
S1	3	("6307268" "6342733" "6368967"). PN.	USPAT	OR	OFF	2006/01/18 13:21
S2	8	("5504017" "5614764" "6004827" "6306732" "6320391" "6498384" "6570181" "6831365").PN.	USPAT	OR	OFF	2006/01/18 13:21
S3	9	("5010024" "5156909" "5504017" "5550405" "5973402" "6037795" "6174743" "6191481" "6221794").PN.	USPAT	OR	OFF	2006/01/18 13:22
S4	2	("5640097" "5663651").PN.	USPAT	OR	OFF	2006/01/18 13:23
S5	5	((("6396751") or ("6617180")) or ("6897475") or ("6934206") or ("20050224792")).PN.	US-PGPUB; USPAT	OR	OFF	2006/01/18 13:23

EAST Search History

S6	1	("20050224792").PN.	US-PGPUB; USPAT	OR	OFF	2006/04/27 13:01
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EAST Search History

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EAST Search History

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S22	4	S13 and width and copper	US-PGPUB; USPAT; USOCR	OR	OFF	2006/04/27 14:13
S23	13	S13 and width and thickness	US-PGPUB; USPAT; USOCR	OR	OFF	2006/04/27 14:13
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EAST Search History

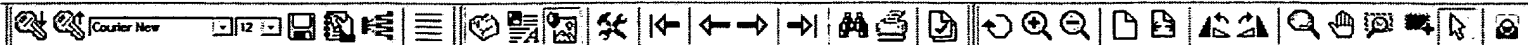
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S29	909	(test near structure) and "324"/\$. ccls.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/04/27 14:16
S30	1066	(test near structure) and "257"/\$. ccls.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/04/27 14:16
S31	1064	(test near structure) and "438"/\$. ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2006/04/27 14:17
S32	118	S29 and S30	US-PGPUB; USPAT; USOCR	OR	ON	2006/04/27 14:17
S33	457	S31 and S30	US-PGPUB; USPAT; USOCR	OR	ON	2006/04/27 14:17
S34	50	S31 and S30 and S29	US-PGPUB; USPAT; USOCR	OR	ON	2006/04/27 14:18
S35	15	S27 and S34	US-PGPUB; USPAT; USOCR	OR	ON	2006/04/27 14:25
S36	9	("5010024" "5156909" "5504017" "5550405" "5973402" "6037795" "6174743" "6191481" "6221794").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/04/27 14:25
S37	55	(cross near2 test near structure)	USPAT	OR	OFF	2006/04/27 16:24
S38	0	(cross near test near structure)	USPAT	OR	ON	2006/04/27 16:24
S39	20	("3335340" "4516071" "5561373").PN. OR ("6057171"). URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/04/27 16:45

EAST Search History

S40	41	(US-20050224792-\$).did. or (US-6055858-\$ or US-5990567-\$ or US-5949547-\$ or US-6057171-\$ or US-6111269-\$ or US-6559475-\$ or US-6087189-\$ or US-5835161-\$ or US-4672314-\$ or US-5838161-\$ or US-4855253-\$ or US-4896108-\$ or US-6563320-\$ or US-5663651-\$ or US-3650020-\$ or US-6650129-\$ or US-6747445-\$ or US-6822437-\$ or US-6894520-\$ or US-6343370-\$ or US-6995392-\$ or US-5963784-\$ or US-6403389-\$ or US-3974443-\$ or US-5608285-\$ or US-4347479-\$).did. or (US-6362638-\$ or US-4386459-\$ or US-6144040-\$ or US-6525548-\$ or US-6022750-\$ or US-5552718-\$ or US-5640097-\$ or US-6822260-\$ or US-6815319-\$ or US-6790685-\$ or US-6620635-\$ or US-6600333-\$ or US-5561373-\$ or US-4516071-\$).did.	US-PGPUB; USPAT	OR	OFF	2006/04/27 16:56
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S46	0	(test near structure) and damascene and width and thickness and copper	EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 17:24

EAST Search History

S47	130	(test near structure) and damascene and width and thickness and copper	US-PGPUB; USPAT	OR	ON	2006/04/27 17:24
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S49	111	S47 not S44	US-PGPUB; USPAT	OR	ON	2006/04/27 17:40
S50	81	("5504017" "5614764" "5661345" "6004827" "6191481" "6306732" "6320391" "6498384" "6570181" "6725433" "6747445" "6831365" "6908847")".PN"	US-PGPUB; USPAT	OR	ON	2006/04/27 17:41
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S52	68	S50 not S51	US-PGPUB; USPAT	OR	ON	2006/04/27 17:45
S53	7	van near der near Pauw near test near structure	USPAT	OR	OFF	2006/04/27 18:31
S54	7	(van near der near Pauw near test near structure) and wafer	USPAT	OR	OFF	2006/04/27 18:32



U.S. Patent

Nov. 7, 2000

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6,144,040

FIG. 2A

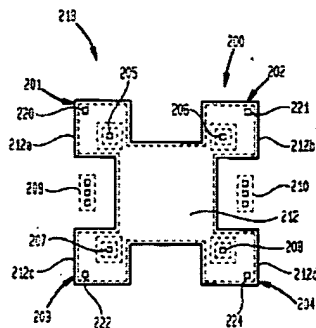
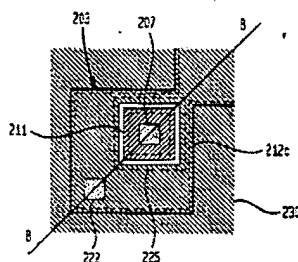


FIG. 2B



In one embodiment, the inner and outer isolation structures of the van der Pauw semiconductor test structure comprise field oxide. Additionally, the field oxide has openings formed therein through which each of the first and second contacts extend to connect to the first and second diffusion regions, respectively. The first and second contacts are metal contacts. The van der Pauw test structure further includes a dielectric layer formed over each of the inner and outer isolation structures that has openings formed therein through which each of the first and second contacts extend to connect to each of the first and second diffusion regions, respectively.

Drawing Description Text - DRTX (3):

FIG. 1A illustrates a top view of a prior art van der Pauw test structure that may be used to determine the resistivity of an N-tub measured under a field oxide;

Drawing Description Text - DRTX (4):

FIG. 1B illustrates an enlargement of the third sub-test structure showing enhanced detail for the prior art van der Pauw test structure of FIG. 1A;

Drawing Description Text - DRTX (6):

FIG. 2A illustrates a top view of an embodiment of a van der Pauw test structure that may be used to determine the resistivity of a first-tub measured under a second-type diffusion area;

Drawing Description Text - DRTX (7):

FIG. 2B illustrates an enlargement of the third sub-test structure showing enhanced detail for the van der Pauw test structure of FIG. 2A;

Drawing Description Text - DRTX (11):

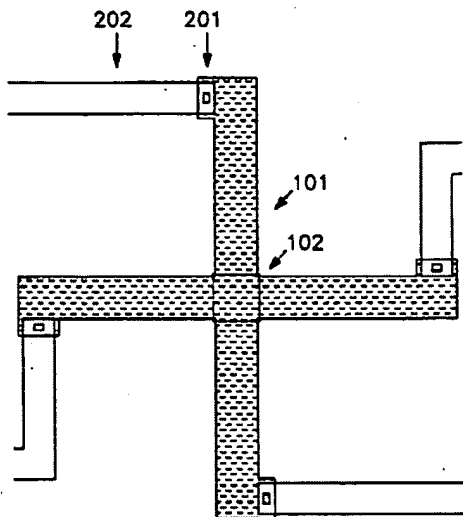
FIG. 3A illustrates a top view of an alternate embodiment of a van der Pauw test structure that may be used to determine the resistivity of a first-tub measured under a gate structure;

Detailed Description Text - DETX (2):

Details Text Image HTML KWIC

U.S. Patent Jul. 11, 2000 Sheet 4 of 4 6,087,189

FIG. 2b



US-PAT-NO: 6087189
 DOCUMENT- US 6087189 A
 IDENTIFIER:
 TITLE: Test structure for monitoring overetching of silicide during contact opening

Abstract Text - ABTX (1):

For the contact opening in advanced IC processing, it becomes critical to monitor the degree of overetching of the thin silicide layer and also to obtain the etching rate of the silicide layer. A method is disclosed which will allow the electrical measurements of the sheet resistance of the exposed (by the contact etch) silicide layer, thus allowing electrical measurements to the integrity as well as the thickness of the remaining silicide layer. A main feature of the disclosed test method is a modification of the conventional van der Pauw test structure, or of the cross-bridge structure (which will allow electrical measurement of the line width, in addition to the sheet resistance information). Contrary to the conventional van der Pauw structure or cross-bridge structure where the contact opening pattern is designed to expose only the specific areas needed for allowing electrical connection to the four measurement pads, the contact opening mask is designed to expose some or all of the van der Pauw or cross-bridge structure, thus allowing the electrical measurement of the degree of silicide overetching during contact opening. The disclosed test method and corresponding structure can be applied as an on-wafer process monitor tool following the complete normal process flow, thus serving as a convenient on-wafer monitor.

Drawing Description Text - DRTX (2):

FIG. 1a schematically shows van der Pauw test structure

Detailed Description Text - DETX (10):

The principle of "the Electrical Detecting Method in Monitoring the Intactness of the Silicide layer on Source/Drain/Gate during Contact Layer Opening" of this invention is simple and practical. It is derived from the conventional van der Pauw test structure as shown in FIG. 1a or the cross-bridge structure as shown in FIG. 1b. Based on 1978 J. Electrochemical Society, 125 Issue, pp.645-650 and pp. 650-654 as shown in FIG. 1a

Disclosed by M. C. P. and others

Details | Toc | Image | HTML | KWIC

U.S. Patent May 1, 2000 Sheet 5 of 12 6,057,171

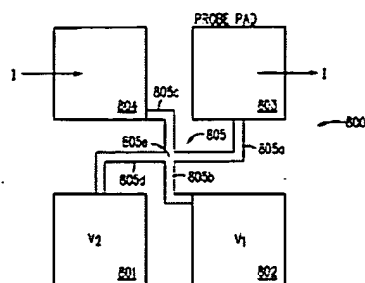
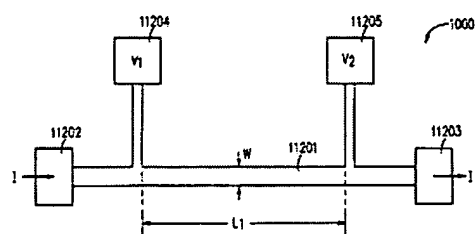
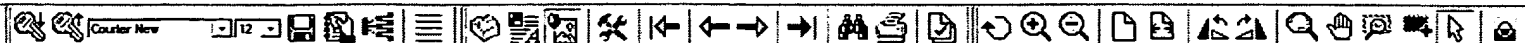
FIG. 8
(PRIOR ART)

FIG. 10

US-PAT-NO: 6057171
DOCUMENT- US 6057171 A
IDENTIFIER:
TITLE: Methods for determining on-chip interconnect process parameters

Drawing Description Text - DRTX (9):

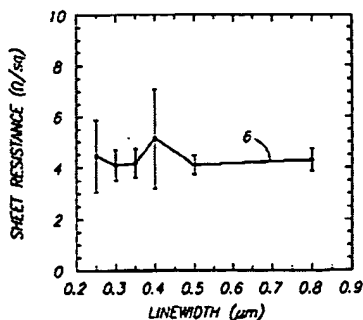
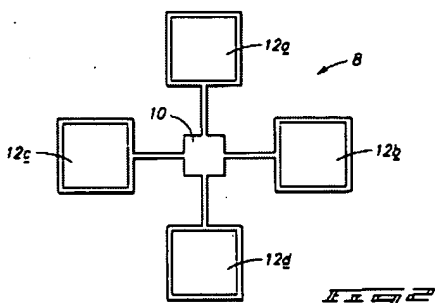
FIG. 8 shows a van der Pauw test structure 800 of the prior art for determining a sheet resistivity for a conductor layer.



L16: (7) van near der... | US 5963784 | Tag: S,P,T1 | Doc: 777 | "Full" 2/14

L16: (7) van near der... | US 5963784 A | Tag: S,P,T1 | Doc: 777 | Format

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FIG. 2
PRIOR ARTUS-PAT-NO: 5963784
DOCUMENT- US 5963784 A
IDENTIFIER:

See image for Certificate of Correction

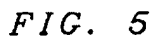
TITLE: Methods of determining parameters of a semiconductor device and the width of an insulative spacer of a semiconductor device

Detailed Description Text - DETX (8):

Referring to FIG. 2, a Van der Pauw test structure 8 may be utilized for providing sheet resistance measurements for determining device parameters. The Van der Pauw structure 8 comprises a plurality of pads 12a-12d coupled with a test substrate 10, such as a semiconductor substrate. The Van der Pauw structure 8 is utilized to determine the sheet resistance of the semiconductor test substrate 10. A plurality of pads 12a-12d are coupled with the semiconductor test substrate 10 as shown in FIG. 2. To determine the sheet resistance of the semiconductor test substrate 10, a voltage differential is applied across first pad 12a and second pad 12b. A current source is coupled with third pad 12c and is utilized to supply a current to the pad.

Details Text Image HTML KWIC

DOCUMENT- US 20060019414 A1
IDENTIFIER:
TITLE: Wiring structure to minimize stress induced void
formation



[0005] Void detection in metallization patterns is accomplished in U.S. Pat. 5,504,017 by passing a current across a metal layer to generate a hot spot in a barrier layer adjacent to the void. The hot spot is detected by an infrared technique or by coating a liquid crystalline material on the metal and measuring a calorimetric response.

[0006] A test structure is disclosed in U.S. Pat. No. 6,004,927 in which a metal runner is formed on a substrate. After a sintering process, a dielectric layer is removed to reveal bumps on the runner. When bump concentration at a given location is more than 20% higher than the average bump density, long term failure is predicted at that site.

{0007} In U.S. Pat. No. 6,499,384, a test structure is fabricated on a semiconductor wafer and comprises a first layer of metal that has second and fourth channels which are connected in series by vias with first, third, and fifth channels in a second metal layer. Openings in a capping layer allow the first and fifth channels to be probed for resistance and compared to a calibration measurement.

[0005] U.S. Pat. No. 6,320,391 describes a long narrow test conductor that is connected to an extension metal conductor on each end by a plurality of vias that avoids a current crowding effect when placing only one via at each end of the test conductor. The test structure is compatible with a high stressing current.

[0009] In U.S. Pat. No. 6,570,181, a reliability test structure is

59	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6935578 B1	20041228	6	methods for evaluating Test structure for differentiating the line and	439
60	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6768323 B1	20040727	13	System and method for determining location of	324

U.S. Patent Oct. 3, 1989 Sheet 1 of 2 4,871,962

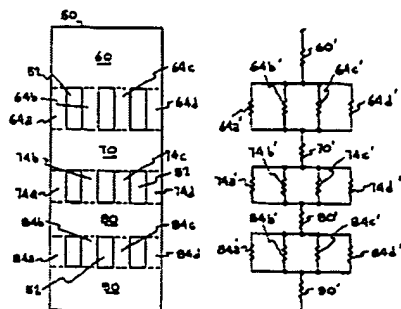


FIG. 1A

FIG. 1B

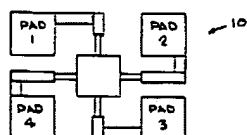


FIG. 2

US-PAT-NO: 4871962
 DOCUMENT-IDENTIFIER: US 4871962 A
 TITLE: Method for measuring the size of vias

US Reference Patent Number - URPN (2):

4516071

Details	Text	Image	HTML	KWIC	
50	<input type="checkbox"/>	<input type="checkbox"/>	US 6921672 B2	20050726	57
51	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 5952674 A	19990914	11
52	<input type="checkbox"/>	<input type="checkbox"/>	US 20020098681 A1	20020725	11
4					

US 6921672 B2 20050726 57 Test structures and methods for inspection of
 US 5952674 A 19990914 11 Topography monitor
 US 20020098681 A1 20020725 11 Reduced electromigration and stressed induced migration

U.S. Patent May 7, 1985 Sheet 1 of 6 4,516,071

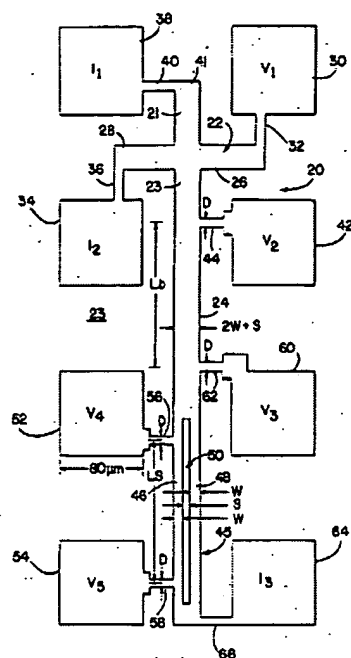


FIG. 1

US-PAT-NO: 4516071
 DOCUMENT- US 4516071 A
 IDENTIFIER:
 TITLE: Split-cross-bridge resistor for testing for proper fabrication of integrated circuits

US Patent No. - PN (1):

4516071

Details	Text	Image	HTML	KWIC
49	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
50	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>
51	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

49	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 4835466 A	19890530	17	detecting vertically	324/
50	<input type="checkbox"/>	<input type="checkbox"/>	US 6921672 B2	20050726	57	Apparatus and method for detecting spot defects in	438/
51	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 5952674 A	19990914	11	Test structures and methods for inspection of	257/

U.S. Patent Sep. 16, 2003 Sheet 2 of 8 US 6,620,635 B2

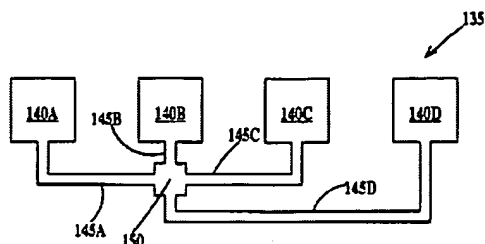


FIG. 3

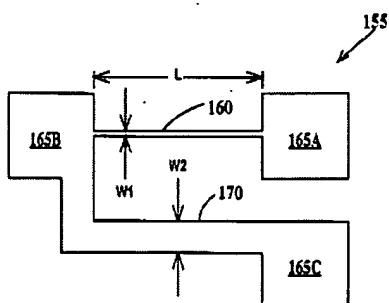


FIG. 4

US-PAT-NO: 6620635
DOCUMENT- US 6620635 B2
IDENTIFIER:

TITLE: Damascene resistor and method for measuring the width of same

Abstract Text - ABTX (1):

A linewidth measurement structure for determining linewidths of damascened metal lines formed in an insulator is provided. The linewidth measurement structure including: a damascene polysilicon line formed in the insulator, the polysilicon line having an doped region having a predetermined resistivity.

TITLE - TI (1):

Damascene resistor and method for measuring the width of same

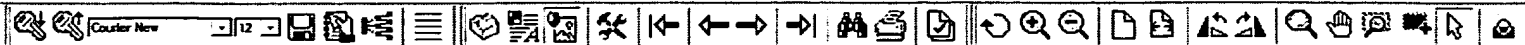
Brief Summary Text - BSTX (2):

The present invention relates to the field of linewidth measurement; more specifically, it relates to a semiconductor damascene resistor and a method of forming and measuring the width of the resistor.

Brief Summary Text - BSTX (7):

A faster technique is to measure the linewidth electrically. In electrical linewidth measurement the sheet resistance of a conductive material is determined using a test structure, then a known current is passed along second test structure having a line fabricated from the same material. If the line is of known length and thickness, then the linewidth can be calculated from the sheet resistance and the voltage drop along the known length of line. Linewidth measurement of a line formed by subtractive means is well known. To measure a damascene line is more challenging. In a damascene process, a conductive line is formed by etching a trench in an insulator, depositing a layer of conductive material on the top surface of the insulator of a thickness sufficient to fill the trench and then chemical-mechanical-polishing (CMP) the excess conductive material until the top surface of the insulator is exposed again.

Details	Text	Image	HTML	KWIC
46	<input checked="" type="checkbox"/>	US 6150669 A	20001121	7
47	<input checked="" type="checkbox"/>	US 5247262 A	19930921	6
48	<input checked="" type="checkbox"/>	US 5051690 A	19910924	22
				line width of electrode and
				Combination test structures
				for in-situ measurements
				257/
				Linewidth micro-bridge test
				structure
				324/
				Apparatus and method for
				detecting vertically
				324/



Tagged | US 6790685 | Tag: S.P.T1 | Doc: 37/60 | "Full" 5/14 (Total images 14)

Tagged | US 6790685 B2 | Tag: S.P.T1 | Doc: 37/60 | Format: KWIC

U.S. Patent Sep. 14, 2004 Sheet 4 of 6 US 6,790,685 B2

FIG. 6

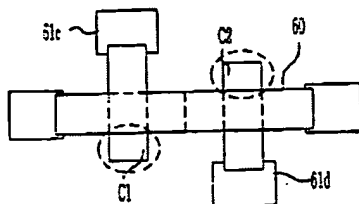
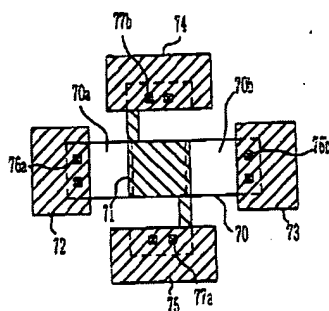


FIG. 7



US-PAT-NO: 6790685

DOCUMENT- US 6790685 B2

IDENTIFIER:

TITLE: Method of forming a test pattern, method of measuring an etching characteristic using the same and a circuit for measuring the etching characteristic

US Document Identifier - DID (1):

US 6790685 B2

Details	Text	Image	HTML	KWIC	
44	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 4978923 A	19901218	14
45	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 5834795 A	19981110	7
46	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6150669 A	20001121	7

Electrical measurements of the profile of semiconductor 324/
 Test pattern for measuring line width of electrode and 257/
 Combination test structures for in-situ measurements 257/

U.S. Patent Feb. 8, 2000 Sheet 3 of 4 6,022,750

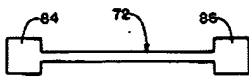


FIGURE 5

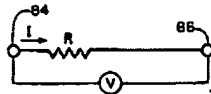


FIGURE 5A

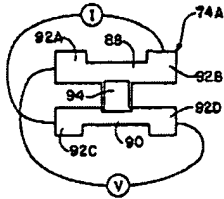


FIGURE 6

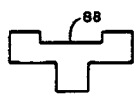


FIGURE 6B

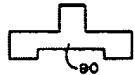


FIGURE 6C

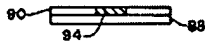


FIGURE 6A

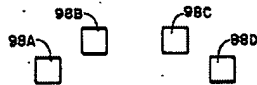


FIGURE 7A

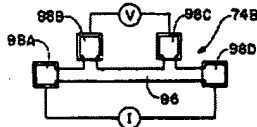


FIGURE 7



FIGURE 7B

US-PAT-NO: 6022750
 DOCUMENT- US 6022750 A
 IDENTIFIER:
 TITLE:

Method for fabricating semiconductor interconnect having test structures for evaluating electrical characteristics of the interconnect

US Document Identifier - DID (1):

US 6022750 A

Details	Text	Image	HTML	KWIC
40	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
41	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
42	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

No.	Pub. No.	Pub. Date	Pub. Title	Pub. No.
40	US 5561373 A	19961001	Method and device for detecting electrostatic	324/
41	US 4516071 A	19850507	Split-cross-bridge resistor for testing for proper	324/
42	US 4399205 A	19830816	Method and apparatus for determining photomask	430/

U.S. Patent Mar. 26, 2001 Sheet 2 of 5 US 6,362,638 B1

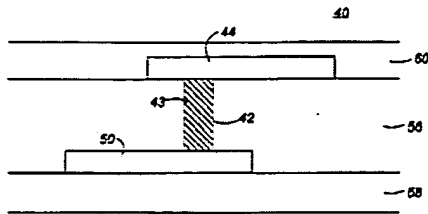


FIG. 3
(PRIOR ART)

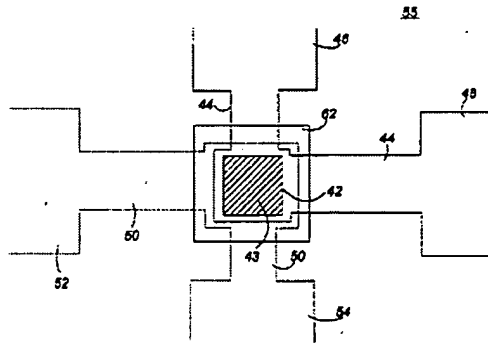


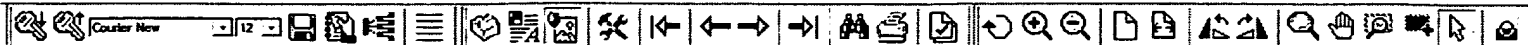
FIG. 4

US-PAT-NO: 6362638
DOCUMENT-
IDENTIFIER: US 6362638 B1
TITLE: Stacked via Kelvin resistance test structure for measuring contact anomalies in multi-level metal integrated circuit technologies

US Document Identifier - DID (1):

US 6362638 B1

Details	Text	Image	HTML	KWC
36	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6915319 B2	20041109
37	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6790685 B2	20040914
38	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6620635 B2	20030916
structure with embedded Damascene resistor and method for measuring the				
Method of forming a test pattern, method of measuring				
Damascene resistor and method for measuring the				

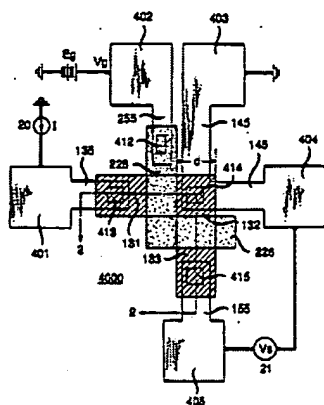


Tagged | US 4896108 | Tag: S.P.T1 | Doc: 12/60 | "Full" 4/11 (Total images 11)

Tagged | US 4896108 A | Tag: S.P.T1 | Doc: 12/60 | Format: KWC

U.S. Patent Jan. 23, 1990 Sheet 3 of 3 4,896,108

FIG. 4



US-PAT-NO: 4896108
 DOCUMENT- US 4896108 A
 IDENTIFIER:

See image for Certificate of Correction

TITLE: Test circuit for measuring specific contact resistivity
 of self-aligned contacts in integrated circuits

US Document Identifier - DID (1):

US 4896108 A

Details	Text	Image	HTML	KWC
20	<input checked="" type="checkbox"/>	US 6343370 B1	20020129	58
21	<input checked="" type="checkbox"/>	US 6995392 B2	20060207	7
22	<input checked="" type="checkbox"/>	US 20050224792 A1	20051013	7
capacitance measurement				
Apparatus and process for pattern distortion detection				
Test structure for locating electromigration voids in				
Novel test structure for speeding a stress-induced				

U.S. Patent Aug. 8, 1989 Sheet 2 of 4 4,855,253

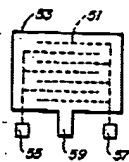


FIG. 4a

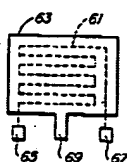


FIG. 4b

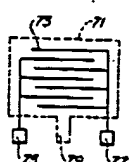


FIG. 4c

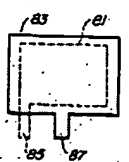


FIG. 4d

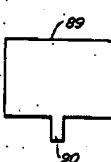


FIG. 4e

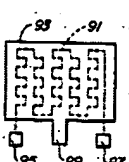


FIG. 4f

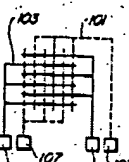


FIG. 4g

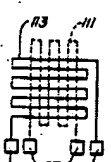


FIG. 4h

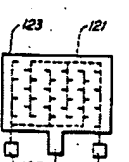


FIG. 4i

US-PAT-NO: 4855253
 DOCUMENT-IDENTIFIER: US.4855253 A
 TITLE: Test method for random defects in electronic microstructures

US Document Identifier - DID (1):

US 4855253 A

Details	Text	Image	HTML	KWIC
19	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6994520 B2 20050517 41 with slotted feeder lines to Semiconductor device and capacitance measurement 324/
20	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6343370 B1 20020129 58 Apparatus and process for pattern distortion detection 716/
21	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6995392 B2 20060207 7 Test structure for locating electromigration voids in 257/

U.S. Patent

Nov. 17, 1998

Sheet 4 of 4

5,838,161

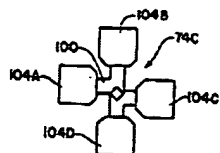


FIGURE 8

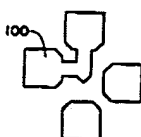


FIGURE 8A

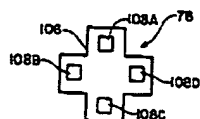


FIGURE 9

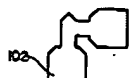


FIGURE 9B

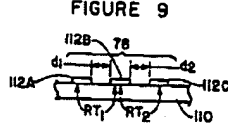


FIGURE 10

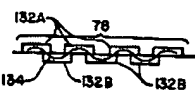


FIGURE 10A

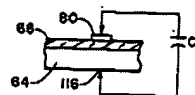


FIGURE 11

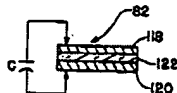


FIGURE 12

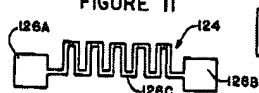


FIGURE 13

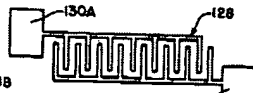


FIGURE 14

US-PAT-NO: 5838161

DOCUMENT- US 5838161 A

IDENTIFIER:

TITLE: Semiconductor interconnect having test structures for evaluating electrical characteristics of the interconnect

US Document Identifier - DID (1):

US 5838161 A

Details	Text	Image	HTML	KWC
18	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	structure and method
19	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	Interconnect test structure with slotted feeder lines to semiconductor device and capacitance measurement
20	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	Apparatus and process for pattern distortion detection

(12) United States Patent
Lin et al.

(20) Patent No.: US 6,835,578 B1
(45) Date of Patent: Dec. 28, 2004

(34) TEST STRUCTURE FOR DIFFERENTIATING THE LINE AND VIA CONTRIBUTION IN STRESS MIGRATION

6,835,578 A 12/2000 Ryan 438/6
6,835,578 B1 12/2002 Ryan et al. 257/62

* cited by examiner

(35) Inventors: Li-To S. Lin, Brian Chen (TW);
Chen-Chia Hsin, Taipei (TW)

Primary Examiner—Matthew Smith
Assistant Examiner—Yvonne V. Yerrico
(74) Attorney Agent or Firm—Haynes and Boone, LLP

(73) Assignee: Taiwan Semiconductor Manufacturing Company, Ltd.,
Hsin-Chu (TW)

(57) ABSTRACT

(*) Notice: Subject to any disclaimer, the term of this patent is extended to adjusted under 35 U.S.C. 154(b) by 0 days.

A method of measuring the stress migration of vias, and a test structure, the method comprising the following steps. A metal line having a middle and opposing first and second ends is formed. First and second opposing pads electrically connected to the respective opposing first and second ends of the metal line through respective first and second steps with the structure are formed. A third pad connected to the metal line proximate to the first end by a first via through a first metal extension is formed. A fourth pad connected to the metal line proximate to the second end by a second via through a second metal extension is formed. The first and second vias are equivalent from the respective first and second ends of the metal line. The stress migration of the first via is determined by measuring the sheet resistance between the first pad and the third pad, and/or the stress migration of the second via is determined by measuring the sheet resistance between the fourth pad and the second pad.

(21) Appl. No.: 10/672,438

(22) Filed: Sep. 24, 2003

(51) Int. Cl. H01L 23/46

(52) U.S. Cl. 438/6; 438/6; 438/6; 438/6

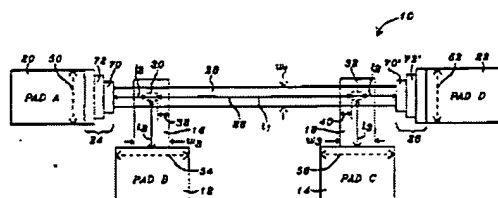
(53) Field of Search 438/6; 438/6; 438/6; 438/6

(54) References Cited

U.S. PATENT DOCUMENTS

6,835,578 A * 12/2000 Ryan 438/6
6,835,578 B1 12/2002 Ryan et al. 257/62

33 Claims, 1 Drawing Sheet



US-PAT-NO: 6835578
DOCUMENT- US 6835578 B1
IDENTIFIER:

See image for Certificate of Correction

TITLE: Test structure for differentiating the line and via contribution in stress migration

Brief Summary Text - BSTX (5):

U.S. Pat. No. 6,804,827 to Ryan describes various test structures with aluminum runners and overlying dielectrics.

US Reference Patent Number - URPN (3):

6004827

US Reference Group - URGP (3):

6004827 19991200 Ryan 438/6

Details	Text	Image	HTML	KWC
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60	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

5,838,161



Details Text Image HTML FULL

ke and method	
connect test structure	324
otted feeder lines to	
ductor device and	324
ance measurement	
us and process for	716
distortion detection	